

Refine Search

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(44 AND 45).PGPB,USPT.	37
(L45 AND L44).PGPB,USPT.	37

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<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u> result set
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L46</u>	L45 and l44	37	<u>L46</u>
<u>L45</u>	(713/151-194)[CCLS]	10671	<u>L45</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L44</u>	lock\$3 near5 read\$3 near5 (memor\$4 or stor\$6 or bank)	2219	<u>L44</u>
<u>L43</u>	L41 and l4	1	<u>L43</u>
<u>L42</u>	L41 and l1	33	<u>L42</u>
<u>L41</u>	"(inaccessible or lock\$5 or "not" near3 access\$5) near5 (stack)	2908	<u>L41</u>
<u>L40</u>	L39 not l34	0	<u>L40</u>
<u>L39</u>	L38 and l1	7	<u>L39</u>
<u>L38</u>	valid near5 logical near5 "1"	330	<u>L38</u>
<u>L37</u>	L33 and l7	0	<u>L37</u>

<u>L36</u>	L33 and l6	0	<u>L36</u>
<u>L35</u>	L33 and l4	0	<u>L35</u>
<u>L34</u>	L33 and l1	8	<u>L34</u>
<u>L33</u>	valid near5 logical near5 "0"	238	<u>L33</u>
<u>L32</u>	l25 not l26	139	<u>L32</u>
<u>L31</u>	L30 and l1	199	<u>L31</u>
<u>L30</u>	(respect\$6 or correspond\$3 or corelat\$3) near8 (register\$1) near8 (bank\$1 or file\$1 or array or group\$4 or plural\$7 or multipl\$7 or stack)	12179	<u>L30</u>
<u>L29</u>	L25 and l7	0	<u>L29</u>
<u>L28</u>	L25 and l6	0	<u>L28</u>
<u>L27</u>	L25 and l4	4	<u>L27</u>
<u>L26</u>	L25 and l2	7	<u>L26</u>
<u>L25</u>	L24 and l1	146	<u>L25</u>
<u>L24</u>	(respect\$6 or correspond\$3 or corelat\$3) near8 (register\$1) near3 (bank\$1 or file\$1 or array or group\$4 or plural\$7 or multipl\$7 or stack)	8874	<u>L24</u>
<u>L23</u>	l18 and l7	0	<u>L23</u>
<u>L22</u>	l18 and l6	0	<u>L22</u>
<u>L21</u>	l18 and l4	1	<u>L21</u>
<u>L20</u>	L19 not l9	12	<u>L20</u>
<u>L19</u>	L18 and l1	35	<u>L19</u>
<u>L18</u>	(index\$3 or indices or point\$3 or bit\$1 or flg\$1) near8 (respect\$6 or correspond\$3 or corelat\$3) near8 (register\$1) near6 (bank\$1 or file\$1 or array or group\$4 or plural\$7 or multipl\$7 or stack)	2337	<u>L18</u>
<u>L17</u>	L16	1495	<u>L17</u>
<u>L16</u>	(index\$3 or indices or point\$3 or bit\$1 or flg\$1) near5 (respect\$6 or correspond\$3 or corelat\$3) near8 (register\$1) near3 (bank\$1 or file\$1 or array or group\$4 or plural\$7 or multipl\$7 or stack)	1495	<u>L16</u>
<u>L15</u>	l8 and l2	253	<u>L15</u>
<u>L14</u>	l8 and l7	0	<u>L14</u>
<u>L13</u>	l8 and l6	0	<u>L13</u>
<u>L12</u>	l8 and l4	1	<u>L12</u>
<u>L11</u>	l2 and l4	4	<u>L11</u>
<u>L10</u>	l8 and l3	6	<u>L10</u>
<u>L9</u>	L8 and l1	23	<u>L9</u>
<u>L8</u>	(index\$3 or indices or point\$3 or bit\$1 or flg\$1) near5 (respect\$6 or correspond\$3 or corelat\$3) near8 (register\$1) near3 (bank\$1 or file\$1 or array or group\$4 or plural\$7 or multipl\$7 or stack)	1495	<u>L8</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L7</u>	(725/6)[CCLS]	61	<u>L7</u>
<u>L6</u>	(902/26)[CCLS]	170	<u>L6</u>
<u>L5</u>	(705/64)[CCLS]	559	<u>L5</u>
<u>L4</u>	(705/50-79)[CCLS]	4823	<u>L4</u>
<u>L3</u>	(712/36, 225)[CCLS]	266	<u>L3</u>

L2 (712/2-300)[CCLS]

11431 L2

DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L1 (smart or credit or charg\$3 or identity or access\$3 or personal or bank\$3)
near2 card\$1

97324 L1

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» Key

IEEE JNL	IEEE Journal or Magazine
IEEE JNL	IEEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEEE CNF	IEEE Conference Proceeding
IEEE STD	IEEE Standard

**1. Design of a parallel vector access unit for SDRAM memory systems**

Mathew, B.K.; McKee, S.A.; Carter, J.B.; Davis, A.;

High-Performance Computer Architecture, 2000. HPCA-6. Proceedings. Sixth International Symposium. 8-12 Jan. 2000 Page(s):39 - 48

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